FPGA based Plank Controller for Active Phased Array Radar

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Abstract:

The paper presents the architecture of Plank Controller for active phased array radar. The design is in-system fully re-configurable FPGA based hardware at the middle level of beam steering hierarchy of conventional phased array antenna. Plank receives the beam steering/timing information from ABCU (Antenna Beam Control Unit) and generates timing and control signals required for 8 no of QTRMs integrated to each Plank in the antenna array. In addition to these functions Plank Controller performs the health status monitoring and provides power Supply to 8 nos of QTRMs. The Plank controller is an innovative product which is a fully inhouse designed, compact, State-of-art technology. Plank controller hardware developed using Xilinx 7 series FPGA, high power compact (brick size) & isolated DC-DC convertors, EMI filters providing isolation from other subsystems including adjacent plank controller, all in one package (i.e. combination of high speed Digital electronics, power electronics, high frequency RF engineering and mechanical engineering through miniaturization with liquid cooling system).

Key Words: Cross-talk, Plank Controller (PLKC), Signal Integrity (SI), Power Integrity (PI), Antenna Beam Control Unit (ABCU), Transmit-Receive (TR) Module,Quad Transmit-Receive Module (QTRM), Thermal Profiling

I INTRODUCTION

In active phase array radar systems, it is desirable to generate and steer antenna beam in space by adjusting the phase of each antenna element feed relative to the others. To perform this beam steering function, it is preferable to have flexible and fully reconfigurable hardware to control of the individual antenna elements. However, practical antenna arrays typically include hundreds, or even thousands, of individual antenna elements, and precise timing and control of these antenna elements is very cumbersome. In addition with restrictions in the antenna array size and bulk cabling requirements for interconnecting the associated control hardware, it is more desirable to have compact, reliable and scalable hardware for Plank Controller (PLKC), which controls 32 antenna elements.

The board is indigenously designed with the vision of developing a generic TRM Controller and fulfilling the power supply requirements of TR modules for all the modern Phased Array Radar applications.

The Plank is a fully indigenous, compact, state-of-art technology with Xilinx latest 7 series FPGA, high power brick size isolated DC-DC convertors, X-Band RF combiners/deviders and installed liquid cooling system, all in one package (i.e. combination of high speed Digital electronics, power electronics, RF engineering and mechanical engineering by size miniaturization with optimum use of sapce and liquid cooling). This makes the design stand unique in all aspects, and hold strategic importance from Phased Array Radar point of view.

II IMPLEMENTATION

Plank Controller hardware shall communicate the control/data/timing signals to each of the external 32 TRMs over rugged mil-grade customized blind mated nano-D connectors. Four TRMs are combined as QTRM and their corresponding signals are routed through one rugged nano-D connector. Eight such customized connectors are incorporated on board.

Being very high power DC-DC convertors and high speed LVDS interface used in the board, innovative techniques are used in the placement/routing and signal integrity of the control/data/timing signals on the PCB.

The complete Plank Controller hardware is enclosed in a ruggedized mechanical cold plate as shown in the figure 1. Since there is liquid cooled system for QTRMs only with no provision of forced air cooling, novel techniques are employed for power dissipation from the board and the complete system is qualified as per the MIL-STD-2164(EC) specifications.

Figure 1: Plank Controller Hardware (mechanical enclosure)

1 Design Requirements/ Salient Features:

i. A 14 layer PCB Stack-Up with Strip line concept is designed to manage the complex routing of 54 nos of LVDS interfase @50Mbps. (ref. Figure2)
ii. FR4-dielectric material is used for the fabrication of the PCB and is qualified as per military standard MIL-PRF-55110H (Mil Grade Class 3 PCB) with group 'B' certification in order to support Radar requirement.
iii. It is developed with a form-factor of 539.2*76.5mm; with constraint of non-uniform available height varies from 6.8mm to 0.0mm. This board is developed compact enough to be an immediate and handy solution for all the modern-day Phased Array Radar applications.
iv. It receives control and command signals from ABCU and provides command and control signals to eight QTRMCs via high speed serial LVDS link. Based on phase gradient (PA, PB), phase values for each TRM is computed and compensated from calibration table.

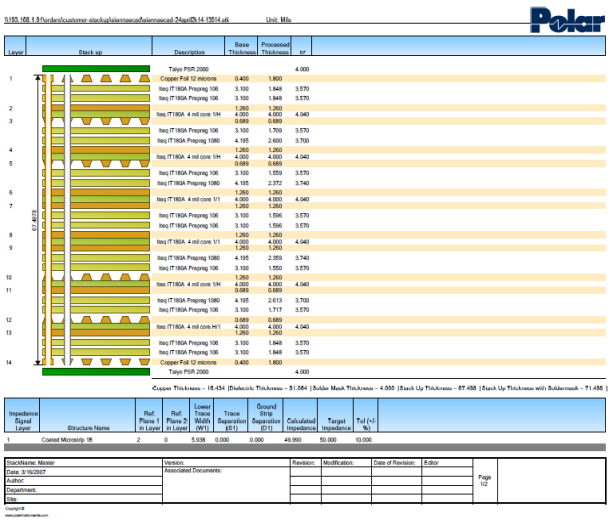

Figure 2: PCB Stack-Up

v. Artex-7 200T FPGA supporting 1040 DSP slices and 19Mb of memory which can support for considerable amount of processing applications along with the genaration of controls for TR Modules.
vi. Artex-7 200T FPGA not only used for generating the phase and amplitude gradiant for TR Modules but also to control the Power supply requirement of QTRMs along with the power supply sequencing.
vii. The user BPI flash provides the flexibility to expand the scope of software applications by storing calibration tables for each of 32 antenna elements separately.
viii. Customized 37-pin Nano-D type Omnetics connectors, with stringent tolerances are usedc control/status communication with blind mated 8 QTRMs.
ix. The board is designed with EMI filters at the inputs of every power supplies so as to nullify the EMI/EMC impact due to nearby RF units.

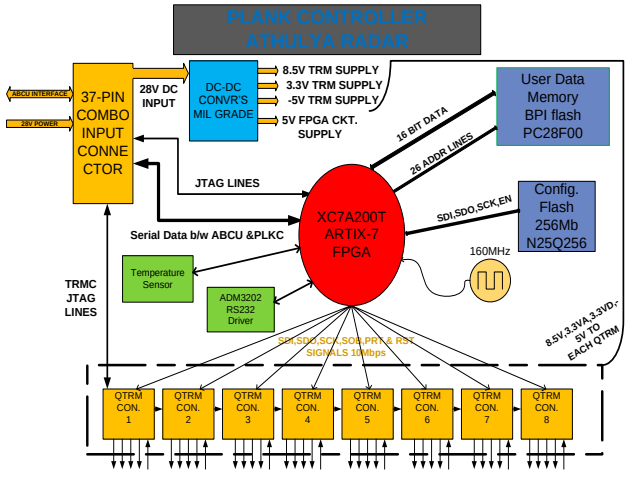

Figure 3: Block diagram of Plank Controller Board

2 Design Plan and Design Realisation

The board is designed in a symmetric fashion with a resourceful Artex-7 FPGA in the centre in order to have minimum trace length from all the critical high frequency operating components. It is interfaced to all the BPI, High-speed transceivers and other peripherals (ref. Figure3). The board is electrically divided into 2 parts with isolated grounds with Digital section of FPGA with associated electronics and High Power DC-DC convertors section. Instead of the traditionally used standard Nano-D and Micro-D type connectors, 37-Pin customized Nano-D and Combo 48-Pin Nicomatic connectors are used in board to interface the 8 QTRMs and Antenna Beam Control Unit (ABCU).

The Plank Controller also has a moderately resourceful Artex-7 FPGA, to which high-speed peripherals are interfaced (ref. Figure3). Considering the high power to be handled by the board the copper planes are sperd over the 4 power layers with 4 individual ground layers for various power supply requirements of QTRMs. Being very minimum avalaible space for the board under the cold plate and power deviders; the components were placed by analising machanical model and its electrical impact symalteneously. Dedicated thermal annlysis and power integrity analysis has been conducted for each of the power layers to cater to withstand the high current requirement. The power integrity comprises of DC-Drop Down Analysis, Decoupling Anlysis and Plane Noise Analysis (ref. Figure 4). The Decoupling Capacitors for corresponding Power Plane can maintain the Target Impedance of 35.42mOhms (8.5V, 12A, 5% of Ripple Voltage) till 200MHz. With the Artex-7 FPGA placed at the centre, the high power DC-DC convertors are paced at both of the end of board to maintain uniform board temperature across its length.
The routing of the BPI and LVDS interfaces to the respective FPGAs is length matched to a tolerance of 25mils to avoid the timing issues observable in FPGA. The Signal Integrity Analysis for Sirial & Parallel Flash, Clock signals and LVDS interfaces has been coducted to avoid the interference/cross talk among high speed signals.

3 Critical-design measures adopted

Owing to the complexity involved, the board realization demanded an innovative approach. While considering the associated thermal and placement and routing issues, it was only after numerous simulations and power estimations- that the realization of the board became feasible. The following are the critical and innovative measures taken during the board realization:

i. The impedance tolerance for the single ended and the differential signals is not allowed to exceed more than 5% of the absolute value i.e., 50 ohms and 100 ohms respectively inclusive of deviations during design of layer stack-up and fabrication.

ii. 54 LVDS lines supporting 50Mbps are routed with utmost care by providing ground shielding along the transceiver lines to avoid cross talk due to adjacent channels and also to make sure that the impact due to adjacent ground shielding on the impedance of the differential transceiver pairs is minimum.

The thermal issues expected in the compact Plank Controller board have been addressed in multiple ways as shown below:

a. by providing appropriate copper grounds in not only power layers but also in the inner signal layers
b. by providing projections for high power dissipating components

c. Most importantly the ground areas on PCB Top and Bottom Layers are made to contact the cold plate and RF deviders which are maintained at 25°C through lequid cooling.
d. The projections for the FPGA digital grounds are not made to contact the PCB casing directly to avoid high current QTRM ground and Digital ground interference. Hence a isolated layers are used for two different grounds.

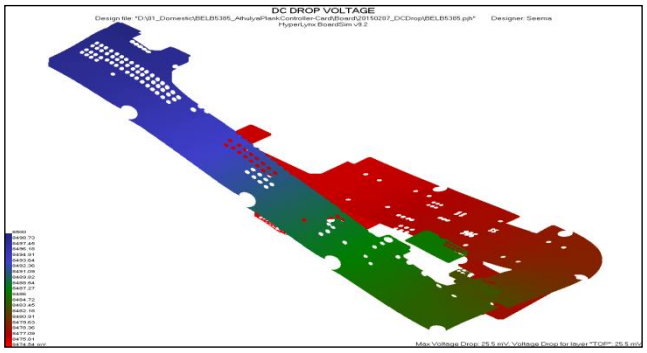

Figure 4: DC-Drop Down Analysis, Decoupling Anlysis and Plane Noise Analysis

h. The placement of the high power dissipating components is planned in a way to have least impact from the other high power dissipating components.

iii. Testing 128 Channels ADCs: A 35 pin RF- connector is placed in every quadrant and of which 32 channels are interfaced to ADC front end circuit. The RF- connector for testing ADC performance is having an inter channel isolation of -100dB. RF connectors are not only used instead of the SMA type connectors to reduce the space occupied but also to facilitate easy testing of all the 128 channels in a quick way. A light weight and cheaper test jig is also designed to make the testing easy and quick. Each Test-jig has 32 SMA connectors to verify all the ADCs performance in a single run. A 1:32 power splitter based test-jig is developed in a way to test an individual ADC or all 32 ADC channels together. ADC digital data of 32 channels can then be captured on the HSDC (High speed Data converter) pro-tool from Texas Instruments and various dynamic parameters can be computed accordingly in a single go.

III ANALYSIS PERFORMED

i. **Thermal**: The thermal profiling of the PCB is performed under the extreme operating conditions (assuming 80% of FPGA critical resources to be utilized for the software application)

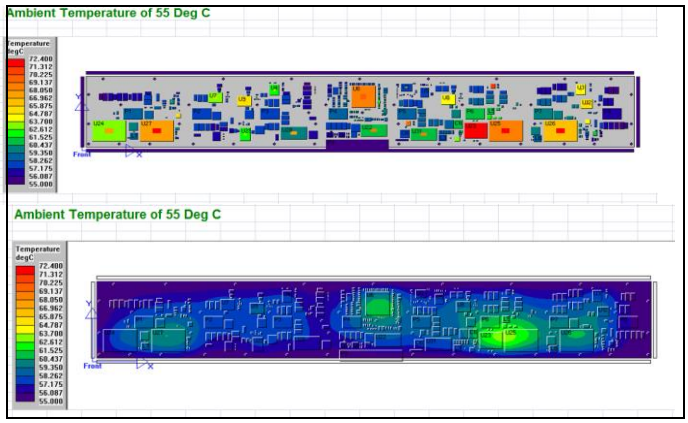

Figure 5: Thermal profiles of the board

ii. **Signal-Integrity:** The design is meticulously analysed to mitigate the ringing effect, crosstalk, ground-bounce, distortion, signal loss and power supply noise.

iii. **Power-Integrity:**

a. DC drop analysis: All the power planes are analysed for the drop in the DC level from source to the load and ensured the drop is within the permissible (as per the recommendations in the datasheet) range
b. Decoupling Analysis: All the power nets are analysed for a wide range of frequencies 1KHz to 200 MHz to make sure the impedance across the band is lower than the target impedance
c. Plane Noise Analysis: Maximum allowable plane noise for all the power nets was observed to be less than 1% (ref figure:4)

IV FUNCTIONAL DESCRIPTION

i. The Plank Controller board receives the control and command signals from ABCU over high speed LVDS lines through combo 48-Pin Nicomatic connector.
ii. Received massage is decoded and based on phase gradient (PA, PB), phase values for each TRM is computed and compensated from calibration table.
iii. The computed and compensated Phase values are sent to each TRM through customized Nano-D connectors over LVDS interface.
iv. The Plank Controller gets +28 V DC power from Power Supply Junction Box and various power supplies (+8.5/7.5 V, +4V analog, +3.3V, -5.0 V) are generated using DC-DC converters required for the TR Modules and other required operating voltages (3.3V,+2.5 V, +1.8 V, 1 V) using voltage regulator for on board operations. (ref Figuer 6)
v. Daisy chain has been implemented for Remote Programming, Monitoring and Debugging all the QTRMs of AAAU without removing the the Plank Controller from AAAU.
vi. Power supply sequencing for all the voltages genarated within the board ahs been implemented through FPGA using low current Photo Resistors (VOM617AT).
vii. There are various features have also been implemented within the board like various Power supplies monitoring using high speed CMOS optocouplers (ACPL074L), Board temperature monitoring using 2°C accurate Digital Temperature Sensor with SPI interface, Input

Power Supply Reverse Polarity Protection etc.

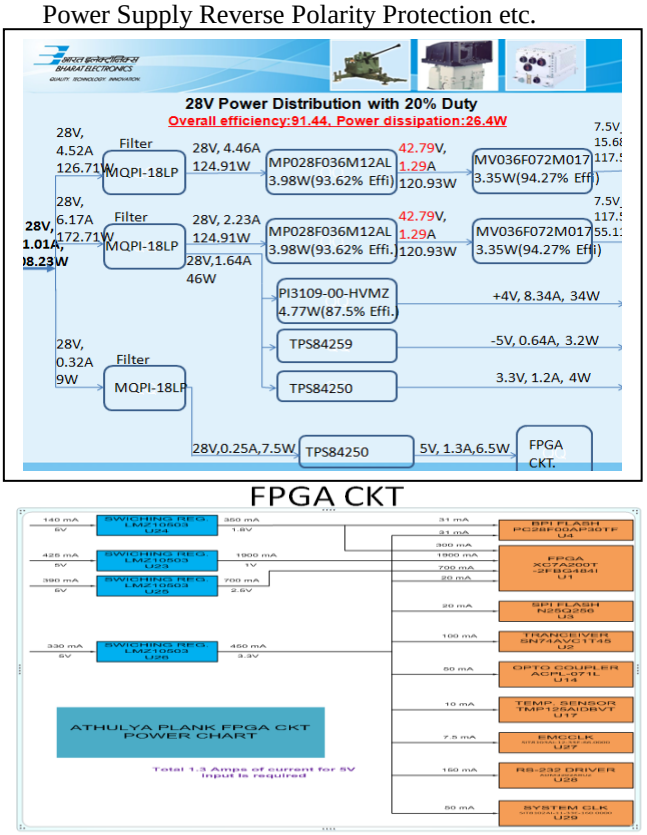

Figure 6: Power Distribution for Plank Controller board

V PERFORMANCE ACHIEVED

i. Thermal, Signal-Integrity and Power-integrity analysis have been meticulously performed in this design owing to which the Board can sustain an overall power efficiency of 91.44% at 308W power input (wit 20% duty at 1ms PRT) without any external cooling. (ref Figure:6)

ii. A very low over all power dissipation of 26.4W on power on with full load.

iii. BPI flash has been verified with storing calibration table writing and reading.

iv. The board developed is verified in the Radar systems like QTRMs and ABCU and the Plank Controller outputs are observed to be compliant with the Radar specifications.

v. 64 nos of Plank Controller boards have been integrated in AAAU and validated with antenna calibration in NFTR by Ms LRDE. (ref Figure:7)

vi. Quality tests like ESS and Reliabilty checks as per Radar requirements have been completed and varified for Plank Controller board.(ref. Figure:8)

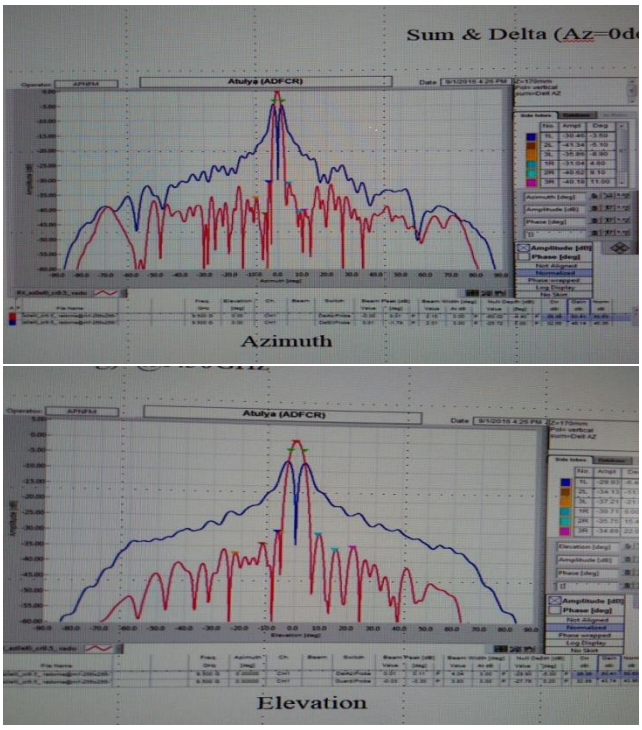

Figure 7: AAAU Antenna Pattern

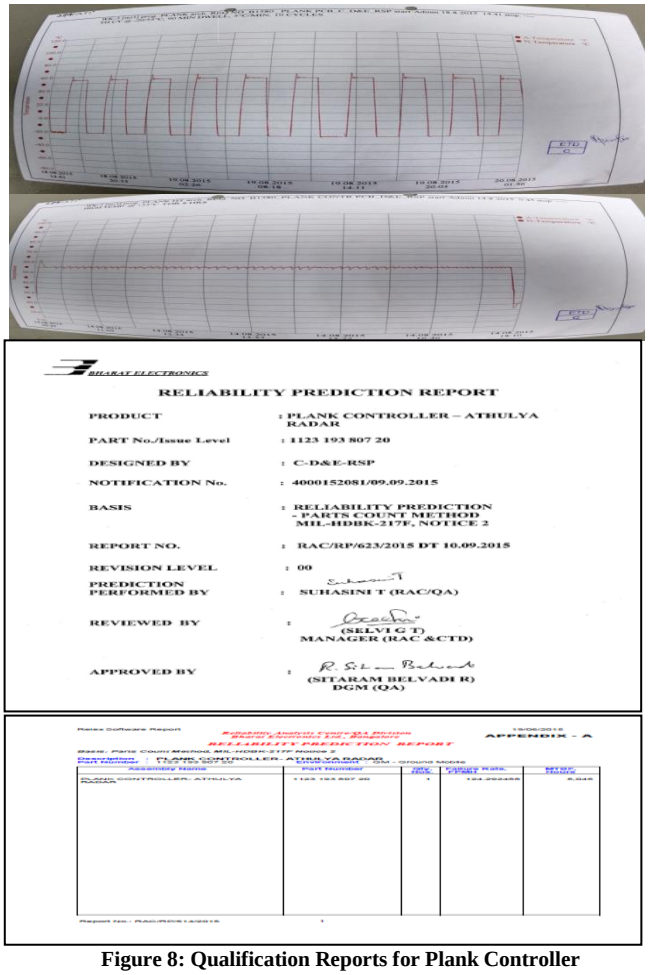

Figure 8: Qualification Reports for Plank Controller

VI SIGNIFICANT FUTURISTIC PROVISIONS

i. With its physical dimensions and ample availability of resources, the Plank Controller comes out as a technology indigenization. The unique design of the board catering to
   a. Computation of Phase values and sending to TR Modules **(Complete)**
   b. Genaration and distribution of Power supplies to TR Modules (**Complete)**
   c. Self Protection, Self Monitring, Power supply sequencing and Remote Programming of QTRMs **(Completed)**

ii. Compact Formfactor with optimum use of space under the stringent thermal constraints (539.2*76.5mm); makes it useful for all the modern active phased array Radar applications.

VII QUALIFICATIONS

i. MIL-PRF-55110H (Mil Grade Class 3 PCB) with group 'B' certification
ii. Dielectric: FR4 per IPC-4101 with min TG 180 Degrees
iii. Solder Mask material meets all the requirements of IPC-SM-840C

VII CONCLUSION

Added to fulfilemtn of high pwer requirement of QTRMs, the high speed LVDS interface and the ample amount of resources available with the use of latest 7-series-Xilinx FPGAs, the physical compactness of the board opens up the scope of large-scale utilisation of the board and makes this State-of-the-art design highly competent with the world class products.

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